RELIABILITY BASED CHARACTERIZATION USING BISECTION

RELATED APPLICATIONS

[0001] The present application claims the benefit of U.S. Provisional Application No. 60/497,972 entitled "RELIABILITY BASED CHARACTERIZATION SYSTEM IN IC/SoS DESIGNS" filed August 25, 2003, the entire contents of which are incorporated herein by reference.

FIELD OF INVENTION

[0002] The present invention generally relates to computer aided methods and tools for designing, simulating, characterizing and verifying integrated circuit (IC) designs, and more particularly to a system and method for verifying and characterizing the noise margin of signals within such designs.

BACKGROUND OF THE INVENTION

[0003] The design of very large-scale integrated (VLSI) circuits using computer aided design (CAD) systems is a very time consuming and computationally intensive process. As the complexity of VLSI circuit design has increased, circuit designers have begun incorporating basic circuit building blocks into circuit designs so that the designers do not need to start from scratch for each design. This design approach is commonly referred to as an intellectual property (IP) based design approach and the basic circuit building blocks are referred to as IP blocks.

[0004] In accordance with system on chip (SOC) technology, a variety of circuit building blocks are incorporated onto a single integrated chip. Each of the building blocks performs a

specific function of an electronic system. The IP building blocks include, but are not limited to, embedded memory, standard cell, I/O devices, analog and system interfaces, etc....

[0005] A timing model including many characterized timing parameters for each IP block that is to be incorporated into a system chip is required by the IC designers. Important timing parameters include setup time, hold time, access time, minimum pulse high and low time, and other I/O pin characteristics. Designers are interested in characterizing and optimizing timing characteristics associated with an IP block design.

[0006] There are two methods of IP block characterization and verification. The first method is based on 'full circuit' simulations. For deep submicron designs, a netlist size of layout-extracted IP blocks could be enormous with a large number of resistors and capacitors. It might be prohibitive to run numerous full circuit simulations with a high-accuracy circuit simulator. The other method is a characterization based on 'critical-path circuit' simulations. Instead of using a full circuit, a small detailed critical circuit including multiple critical paths is used of simulation. The 'critical-path circuits' are built either manually or by software tools for automation, accuracy and performance.

[0007] The simulation results observed during the characterization process are only at the pins of the full circuit or at ports of the 'critical-path circuit'. Reliability issues such as noise margin, glitch, and racing conditions that occur inside the circuit are normally ignored. Accordingly, the timing parameters generated by the simulation may be too optimistic and incorrect.

[0008] Furthermore, the circuit or subcircuit block is viewed as a black-box when the circuit simulation is performed. However, the simulations results observed at the pins cannot detect the above-mentioned reliability issues that can occur inside the circuit. The models based upon simulation and characterization results could be incorrect thereby causing yield and reliability problems.

SUMMARY OF THE INVENTION

[0009] In accordance with the present invention there is provided a method for determining an optimized parameter for a circuit simulation. A circuit path for the simulation is determined, and maximum and minimum optimization parameters are decided. Next, the circuit path is simulated using the maximum optimization parameter. The circuit path is simulated using the minimum optimization parameter and a primary criteria parameter is also calculated from the simulations. The simulations are compared to determine whether the same status (both succeed or both fail) is generated. If the simulations do not indicate the same status, then the optimization parameter is recalculated and the circuit is simulated until the primary criteria parameter converges to a prescribed value.

[0010] The optimization parameter is a setup and hold time for the circuit and the primary criteria parameter is a bisection error of the simulation. In accordance with the present invention, further reliability checks can be performed on the circuit after determining whether the simulations indicate the same status (both succeed or both fail). Typically, the optimization parameter is recalculated by averaging the initial minimum and maximum optimization parameters. In this regard, the recalculated optimization parameter is used to recalculate the primary criteria parameter to determine convergence. If the primary criteria parameter does not converge, then the current optimization parameter is set to the current maximum optimization parameter value for the circuit simulation when the current optimization value and the current minimum optimization parameter do not have the same status (both succeed or both fail). Alternatively, if the primary criteria parameter does not converge and the current optimization value and the current minimum optimization parameter do have the same status (both succeed or

both fail), then the current optimization parameter is set to the current minimum optimization parameter value for the circuit simulation.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] These, as well as other features of the present invention, will become more apparent upon reference to the drawings wherein:

[0012] FIG. 1 is a flowchart illustrating how to determine an optimized parameter for a circuit simulation.

DETAILED DESCRIPTION

[0013] Various aspects will now be described in connection with exemplary embodiments, including certain aspects described in terms of sequences of actions that can be performed by elements of a computer system. For example, it will be recognized that in each of the embodiments, the various actions can be performed by specialized circuits or circuitry (e.g., discrete and/or integrated logic gates interconnected to perform a specialized function), by program instructions being executed by one or more processors, or by a combination of both. Thus, the various aspects can be embodied in many different forms, and all such forms are contemplated to be within the scope of what is described. The instructions of a computer program as illustrated in FIG. 1 for characterizing a circuit can be embodied in any computer readable medium for use by or in connection with an instruction execution system, apparatus, or device, such as a computer based system, processor containing system, or other system that can fetch the instructions from the instruction execution system, apparatus, or device and execute the instructions.

[0014] As used here, a "computer-readable medium" can be any means that can contain, store, communicate, propagate, or transport the program for use by or in connection with the instruction execution system, apparatus, or device. The computer-readable medium can be, for example but not limited to, an electronic, magnetic, optical, electromagnetic, infrared, or semiconductor system, apparatus, device, or propagation medium. More specific examples (a non exhaustive list) of the computer readable-medium can include the following: an electrical connection having one or more wires, a portable computer diskette, a random access memory (RAM), a read only memory (ROM), an erasable programmable read only memory (EPROM or Flash memory), an optical fiber, and a portable compact disc read only memory (CDROM).

[0015] The present invention generally relates to Applicants' co-pending patent applications: "TIMING SOFT ERROR CHECK", Attorney Docket No. 033994-003; "GLITCH AND METASTABILITY CHECKS USING SIGNAL CHARACTERISTICS", Attorney Docket No. 033994-005; and "VERIFICATION AND CHARACTERIZATION OF NOISE MARGIN IN INTEGRATED CIRCUIT DESIGNS", Attorney Docket No. 033994-006, filed concurrently herewith and the entire contents of each application are incorporated herein by reference.

[0016] Referring now to the drawings wherein the showings are for purposes of illustrating preferred embodiments of the present invention only, and not for purposes of limiting the same, Figure 1 is a flowchart illustrating a method of determining an optimized parameter for a circuit simulation. In step 3001, critical-path circuits of full circuits for the circuit simulations are determined for the bisection procedure. The range and precision of the bisection procedure and clock cycle timing need to be decided. In step 3002, the circuit is simulated based upon an initial optimization parameter (OP). For the reliability based characterization illustrated in Figure 1, the OP is the setup time or hold time for the circuit. The initial minimum and maximum OP's are determined by user specified information. In step 3003, the primary criteria parameter (PCP)

is calculated for the initial minimum OP. The PCP is the bisection error for the setup time or hold time. Once the PCP is calculated, then the circuit is simulated in step 3004 for the initial maximum optimization parameter (OP). In step 3005, the current PCP is then calculated for the initial maximum OP.

[0017] In step 3006, the current minimum OP and the current maximum OP are compared to determine if they both fail or succeed. Specifically, if both the current maximum OP and the current minimum OP both indicate the same status (both succeed or both fail), then the process proceeds to step 3007 where the process ends because of a same sign error. However, if both the current minimum OP and the current maximum OP do not indicate the same status, then the process proceeds to step 3008 where other reliability checks on the circuit may be performed. Specifically, the user has the option of performing glitch and metastability checks C1 – C7 as described in applicant's co-pending patent application "GLITCH AND METASABILITY CHECKS USING SIGNAL CHARACTERISTICS", Attorney Docket No. 033994-005, the contents of which are incorporated herein by reference.

[0018] If the user decides not to perform other reliability checks in step 3008, then the process proceeds to step 3009 where the current OP is calculated. Specifically, the current OP is calculated by averaging the current minimum OP and the current maximum OP. After the current OP has been calculated, then the PCP is checked for convergence in step 3010. Specifically, the convergence is determined by whether the bisection error (i.e., PCP) has converged into a bisection precision range which is specified by the user. If the bisection error has converged, then the current OP is saved as the setup and hold time for any subsequent calculations. However, if there is not convergence of the bisection error, then the circuit is simulated again in step 3011 using the current OP calculated in step 3009.

[0019] Once the circuit simulation has been performed, the process proceeds to step 3012 wherein the current OP and the current minimum OP are compared. If both values indicate the same status (i.e., both success or both fail), then the process proceeds to step 3013 wherein the current OP value is set to be the current minimum OP value. Furthermore, the process proceeds to point "A" where in step 3009, the current OP is calculated until convergence occurs.

[0020] However, if in step 3012, the current OP and the current minimum OP values do not indicate the same status, then the process proceeds to step 3014 wherein the current OP is set to be the maximum OP value. Then the process returns to point "A" and step 3009 where the process continues until the bisection error converges. In this respect, the process iteratively repeats to find the optimized setup and hold time.

[0021] It will be appreciated by those of ordinary skill in the art that the concepts and techniques described here can be embodied in various specific forms without departing from the essential characteristics thereof. The presently disclosed embodiments are considered in all respects to be illustrative and not restrictive. The scope of the invention is indicated by the appended claims, rather than the foregoing description, and all changes that come within the meaning and range of equivalence thereof are intended to be embraced.